CLAIMS

What is claimed is:

1. A circuit for evaluating logic level input signals, said circuit comprising:

a pre-charge node;

a clock evaluate node coupled to cause charging of said pre-charge node in response to the logic level of said clock evaluate node;

an output node coupled to said pre-charge node through an inverter logic subcircuit;

a plurality of logic input signal nodes configured to receive logic level input signals; and

multiple pull-down stacks interconnected with said pre-charge node, each said pull-down stack comprising an interstitial node and coupled to discharge said pre-charge node to ground in response to said logic level input signals;

said interstitial node of each said pull-down stack coupled to an interstitial pre-charger device, said interstitial pre-charger device further coupled to deliver charge to said interstitial node in response to the logic level of said clock evaluate node; and

said interstitial node coupled to an interstitial discharger device, said interstitial discharger device gated to ground and coupled to discharge said interstitial node to ground in response to said logic level of said clock evaluate node.

2. The circuit of claim 1 wherein said circuit is a domino-type multiplexing structure logic gate circuit.

3. The circuit of claim 1 comprising a pre-charge field effect transistor (FET) having a gate interconnected with said clock evaluate node and having a channel interconnected between said pre-charge node and a voltage supply.

4. The circuit of claim 1 wherein said pull-down stack comprises a first pull-down FET and a second pull-down FET, said first pull-down FET having a gate connected to a first logic input signal node, said second pull-down FET having a gate connected to a second logic input signal node different from said first logic input signal node, and said first and said second pull-down FETs having respective channels interconnected together in series through said interstitial node.

5. The circuit of claim 4 wherein said interstitial pre-charger device is a pre-charge FET having a gate interconnected with said clock evaluate node and having a channel interconnecting said interstitial node with said voltage supply.

6. The circuit of claim 4 wherein said interstitial discharger device comprises a first FET and a second FET, said first FET having a gate connected to said output node and a channel interconnected in series between said interstitial node and ground through a channel of said second FET, said second FET having a gate connected to said clock evaluate node.

7. The circuit of claim 1 further comprising a keeper FET device having a gate connected to said output node and having a channel interconnected between said pre-charge node and said voltage supply.

8. A method of interstitial pre-discharge in a circuit with multiple pull-down stacks, said method comprising:

providing a circuit comprising:

a pre-charge node;

a clock evaluate node operable to receive a clock evaluate input cycle, said clock evaluate node coupled to said pre-charge node;

said multiple pull-down stacks interconnecting said pre-charge node and ground, said pull-down stacks each comprising an interstitial node; and

said interstitial node of each said pull-down stack coupled to an interstitial discharger device, said interstitial discharger device gated to ground;

operating said circuit in a pre-charge phase of said clock evaluate input cycle, comprising:

pre-charging said pre-charge node and said interstitial nodes; and

keeping devices in said pull-down stacks and said interstitial dischargers in a high impedance (low conductance) state;

operating said circuit in an evaluate phase of said clock evaluate input cycle, comprising:

discharging said pre-charge node to ground through a said pull-down stack; and

discharging said interstitial node to ground through said interstitial discharger device, thereby precluding a charge share event.

9. The method of claim 8 wherein said pre-charging said pre-charge node is performed in response to a logic signal level on said clock evaluate node.

10. The method of claim 8 wherein said pre-charging said interstitial nodes is performed in response to said logic signal level on said clock evaluate node.

11. The method of claim 8 wherein said circuit further comprises a plurality of logic input signal nodes and wherein said maintaining said channels to ground through said pull-down stacks in a high impedance (low conductance) condition is performed in response to logic signal levels on said plurality of logic input signal nodes.

12. The method of claim 11 wherein said discharging said pre-charge node to ground through one of said pull-down stacks comprises causing said channels to ground through said pull-down stack to become conductive.

13. The method of claim 12 wherein said causing said channels to ground through said pull-down stack to become conductive is performed in response to logic signal levels on said plurality of logic input signal nodes and in response to said logic signal level on said clock evaluate node.

14. The method of claim 8 wherein said circuit further comprises an output node coupled to said pre-charge node through an inverter logic subcircuit and wherein said maintaining said channels to ground through said interstitial discharger device in a high impedance (low conductance) condition is performed in response to a logic signal level on said output node and in response to said logic signal level on said clock evaluate node.

15. The method of claim 14 wherein said discharging said interstitial node to ground through said interstitial discharger device comprises transitioning of said channels to ground through said interstitial discharger device to a high conductance condition.

16. The method of claim 15 wherein said transitioning is performed in response to transitioning of said logic signal level on said output node and in response to transitioning of said logic signal level on said clock evaluate node.

17. The method of claim 8 further comprising pre-charging of said interstitial nodes during said pre-charge phase of said clock evaluate input cycle and omitting said pre-charging during said evaluate phase of said clock evaluate input cycle.

18. The method of claim 17 wherein said circuit comprises an interstitial node pre-charger device and wherein said pre-charging and said omitting said pre-charging is performed by transitioning the impedance through a channel of said pre-charger device in response to said logic signal level on said clock evaluate node.

19. A circuit comprising:

means for storing a pre-charge;

means for causing said pre-charge;

means for output coupled to said means for storing said pre-charge;

means for receiving logic level input signals; and

means for discharging to ground said means for storing said pre-charge in response to said logic level input signals;

said means for discharging coupled to means for pre-charging in response to said means for causing said pre-charge; and

said means for discharging coupled to means for pre-discharging in response to said means for causing said pre-charge.